Texas Instruments

# CDCE906/CDCE706 Programming Evaluation Module

## User's Guide

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High Performance Analog/CDC

SCAU017B

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# CDCE906/CDCE706 Programming Evaluation Module

This user's guide explains how to use the CDCE906/CDCE706 programming evaluation module. An easy to use socket is provided on the EVM to make a fast programming of samples or small production quantities possible. There is an another EVM available for the purpose of performance measurements and evaluation, called CDCE906/CDCE706 Performance Evaluation Module.

If you need assistance with this device, email: *clocks_apps@list.ti.com*

## 1 Introduction

The CDCE906/CDCE706 is one of the smallest and powerful PLL synthesizer / multiplier / divider available today. Despite its small physical outlines, the CDCE906/CDCE706 is the most flexible. It has the capability to produce an almost independent output frequency from a given input frequency.

The input frequency can be derived from a LVCMOS, a differential input clock, or a single crystal. The appropriate input waveform can be selected via the SMBus data interface controller.

To achieve an independent output frequency the reference divider M and the feedback divider N for each PLL can be set to values from 1 up to 511 for the M-Divider and from 1 up to 4095 for the N-Divider. The PLL-VCO (voltage controlled oscillator) frequency than is routed to the free programmable output switching matrix to any of the six outputs. The switching matrix includes an additional 7-bit post-divider (1-to-127) and an inverting logic for each output.

The deep M/N divider ratio allows the generation of zero ppm clocks from e.g., a 27-MHz reference input frequency.

The CDCE906/CDCE706 includes three PLLs of those one supports SSC (spread-spectrum clocking). PLL1, PLL2, and PLL3 are designed for frequencies up to 300 MHz and optimized for zero-ppm applications with wide divider factors.

PLL2 also supports center-spread and down-spread spectrum clocking (SSC). This is a proven method to effectively reduce the energy for the selected frequency range. The electro-magnetic interference (EMI) will be significantly reduced. Also, the slew-rate controllable (SRC) output edges minimize EMI noise.

Based on the PLL frequency and the divider settings, the internal loop filter components will be automatically adjusted to achieve high stability and optimized jitter transfer characteristic of the PLL.

The device supports non-volatile EEPROM programming for easy customized applications. It is pre-programmed with a factory default configuration (see Figure 1) and can be re-programmed to a different application configuration before it goes onto the PCB or re-programmed by in-system programming. A different register setting is programmed via the serial SMBus interface.

Two free programmable inputs, S0 and S1, can be used to control for each application the most demanding logic control settings (outputs disable to low, outputs 3-state, power down, PLL bypass, etc).

The CDCE906/CDCE706 has three power supply pins, VCC, VCCOUT1, and VCCOUT2. VCC is the power supply for the device. It operates from a single 3.3-V supply voltage. VCCOUT1 and VCCOUT2 are the power supply pins for the outputs. VCCOUT1 supplies the outputs Y0 and Y1 and VCCOUT2 supplies the outputs Y2, Y3, Y4, and Y5. Both output supplies can be 2.3 V to 3.6 V. The output works even at 1.7V VCCOUT. However, some limitations apply at VCCOUT below 2.3V.

The CDCE906/CDCE706 is characterized for operation from 0°C to 70°C/–40°C to 85°C.

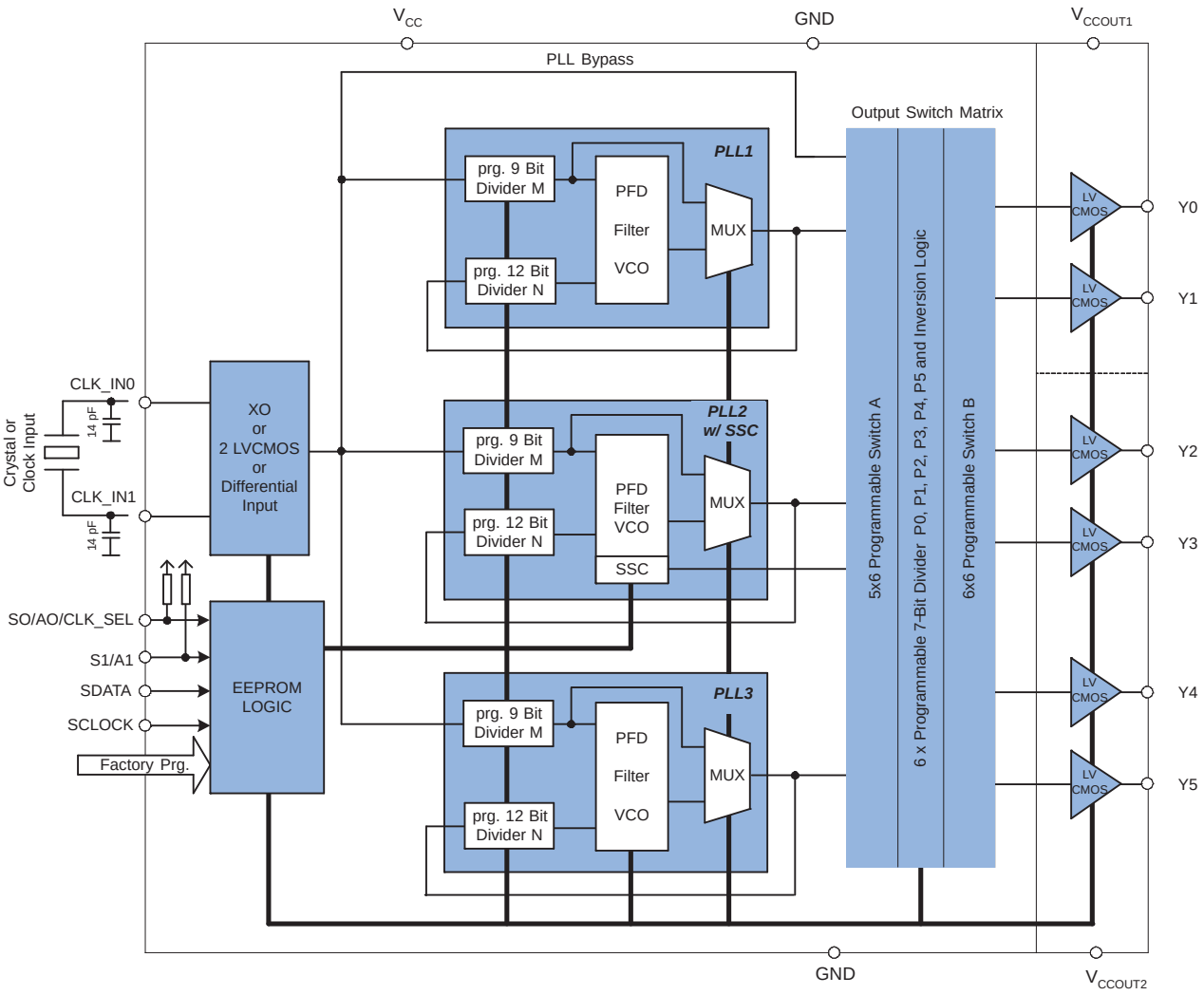


**Figure 1. CDCE906/CDCE706 Functional Block Diagram**

### Related Documentation From Texas Instruments

- *CDCE906, Programmable 3-PLL Clock Synthesizer/Multiplier/Divider* data sheet (SCAS814)
- *CDCE706, Programmable 3-PLL Clock Synthesizer/Multiplier/Divider* data sheet (SCAS815)

## 2 Quick Start

Press the socket in the middle of the EVM down and insert the CDCE906/CDCE706 into the socket. Release the socket to fix the device.

- Connect 3.3 V to P1 and P2
- Make a user defined setup with the *TI Pro Clock* Software (additional information can be found in section 4)
- Connect the EVM with the PC via a parallel cable
- Program the CDCE906/CDCE706 with the *Write* button or the *auto write* function of the *CDCE906-E706 SMBus interface*
- Connect a reference source with the correct input frequency and a minimum swing of 1.32 V to J2
- Check the setup with a high impedance probe at the test points (TP0–TP5 for Y0–Y5)

# 3 EVM Hardware

## 3.1 Board View and Connector Location

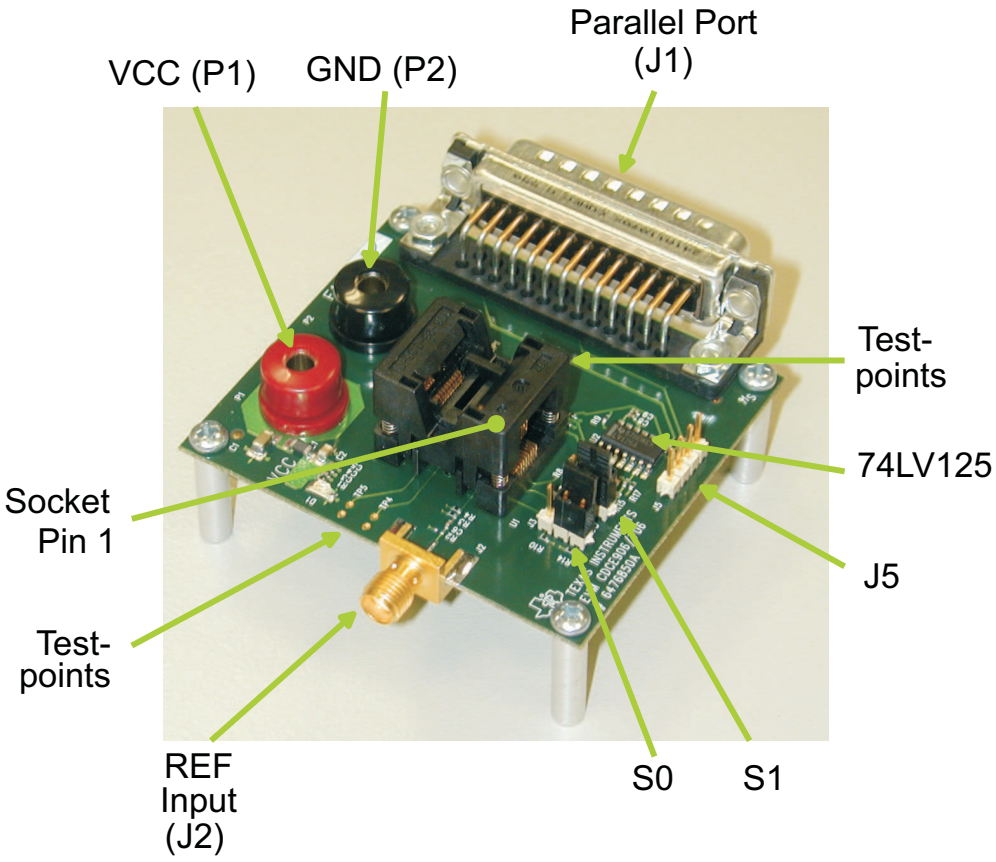


**Figure 2. Board View**

## 3.2 Hardware Configuration

This section describes the board configuration using on-board jumpers and solder-bridges as well as the SMBUS interface.

### 3.2.1 Power Supply (P1, P2)

Use a stabilized external power supply for the EVM board.

- Supply 3.3 V ± 0.3 V on P1
- Connect GND to P2

**WARNING**

**Never supply more than 3.6 V on P1 and P2.**

### 3.2.2 Onboard Jumper (J3 and J4)

Use Jumper J3 to set the user programmable control input S0 to low or high.

Use Jumper J4 to set the user programmable control input S1 to low or high.

*Default setting: J3 and J4 are not used.*

**Note:** S0 and S1 are logic high due to their internal pull-up resistors if J3 and J4 are not used.

### 3.2.3 Programming Interfaces (J1, J5)

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. It follows the SMBus specification Version 2.0, which is based upon the principals of operation of $I^2C$. More details of the SMBus specification can be found at http://www.smbus.org.

Through the SMBus, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the SMBus data interface initialize to their default setting, written in the EEPROM, upon power-up and therefore using this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. There are two ways to program the device externally.

- Connect the parallel port cable to PC and EVM parallel port. This needs the *TI Pro Clock* Software( see section 4)
- By external pattern generator connected to J5 (it is not possible to detect an acknowledge at J5)

**Note:** The shield of the parallel cable should be connected to both cable plugs.

### 3.2.4 Crystal, Differential or LVCMOS Input (J2)

The CDCE906/CDCE706 can use a crystal, a differential, or a LVCMOS input signal. The CDCE906/E706 programming EVM makes possible the functional testing of the device for all three input configurations. This is done by providing a single-ended clock to CLK_IN0. CLK_IN1 is biased to Vcc/2, which offers the option to test the differential input with a single-ended clock provided to J2.

*Default settings: LVCMOS Input at CLK_IN0.*

### 3.2.5 LVCMOS Outputs (TP0 –TP5)

The CDCE906/CDCE706 drives up to six LVCMOS outputs. Test points are available on the board for a functional test after programming the device. Every test point consists of a signal and a GND pad for fast and easy testing with a high impedance probe.

# 4 TI Pro-Clock™

TI Pro-Clock™ is the evaluation software for the CDCE906 and the CDCE706. The software contains the *CDCE906-706 SMBus Interface* and the *CDCE906-706 Programming Assistant*. In the future, the software will be expanded for new devices. The software runs under Windows 2000, XP, and XP*64. A quick installation is required prior to use. See Section 4.4 *Software Installation*.

The *CDCE906-706 SMBus Interface* allows the user direct access to all programmable features of the CDCE906/CDCE706 via the parallel port of the PC.

The *CDCE906-706 Programming Assistant* helps the user to find a proper device setup by choosing the input and output settings.

## *4.1 CDCE906-706 SMBus Interface*

The SMBus Interface is an easy-to-use programming environment and supports many features. It provides direct access to the register and the EEPROM of the CDCE906/CDCE706 and therefore makes evaluation easy.

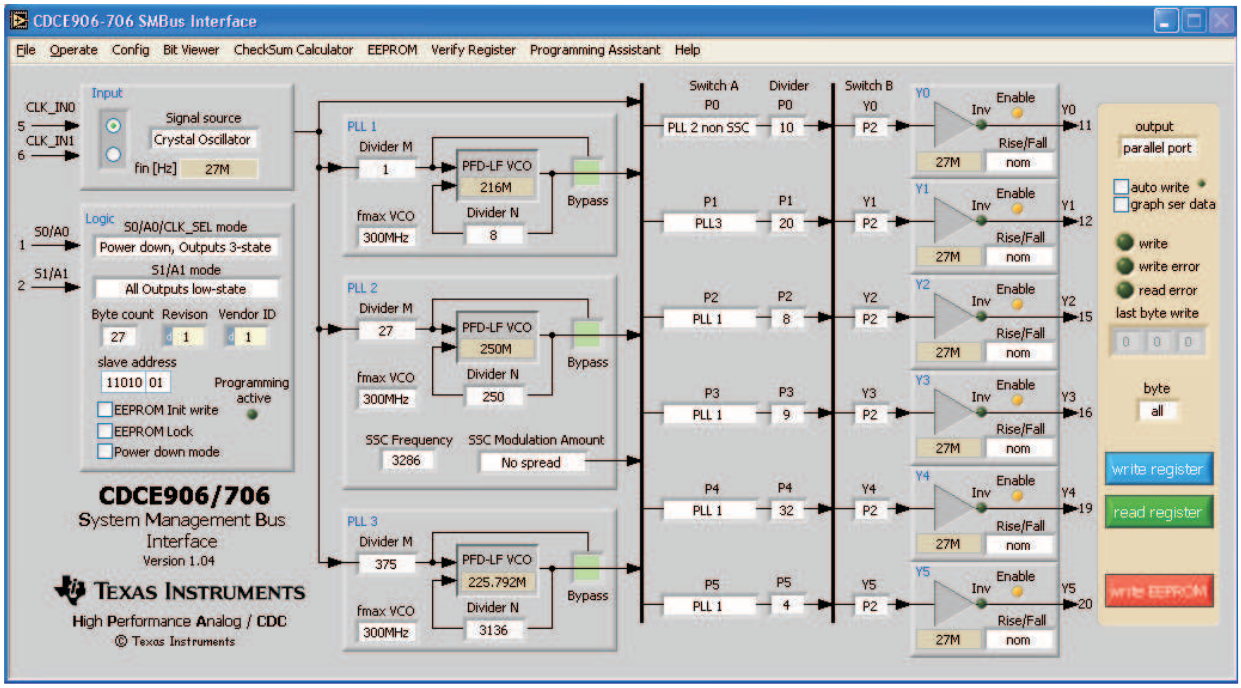


**Figure 3. CDCE906-706 SMBus Interface**

### 4.1.1 Quick Start Instructions

The following steps are necessary for device programming after TI Pro-Clock™ has been installed on your PC:

1. Power up the CDCE706/CDCE906EVM.
2. Connect the EVM and the PC with a parallel cable.
3. Start the TI Pro-Clock™ software.
4. Click the button CDCE906/CDCE706.
5. Make a user-defined setup.
6. Click the *write register* button.

### 4.1.2 Main Screen

The main screen of the CDCE906/CDCE706 SMBUS interface as shown in Figure 3 allows direct control to all programmable features of the CDCE906/CDCE706. All programmable PLL parameters, like divider settings, SSC settings as well as all input and output settings, can be controlled. Clicking the *write register* button transfers the setup to the CDCE906/CDCE706EVM. The parameter byte selects if the whole setup (all bytes) or only the selected byte will be updated in the CDCE906/CDCE706 control register.

By selecting *auto write* in the upper right corner, the CDCE906/CDCE706 SMBus control register gets an update after each change in the setup of the *CDCE906-706 SMBus Interface*. If *graph ser data* is selected, the bit pattern of SCLK and SDATA is shown on a screen.

Click *read register* to load the current control register setup of the CDCE906/CDCE706 into the SMBus Interface. The *write EEPROM* button updates the CDCE906/706 control register and writes the updated control register contents into the EEPROM.

After the SSC settings were changed, PLL 2 must get a reset by setting the PLL into bypass mode for a short time. This is done automatically by the SMBus interface. Due to this, there will be multiple write cycles on the SMBUS after pressing the *write register* or *write EEPROM* button.

A yellow *write* LED indicates an active writing cycle. If the LEDs *write error* or *read error* are switching from green to red, a write/read error occurred. Check the EVM and the parallel cable and try again.

A *Bit Viewer* is available in the menu bar. This feature shows the current setup of the SMBus Interface bit per bit. This allows an easy evaluation of the register setting that is currently set in the SMBus interface.

It is possible to lock the EEPROM permanently. This avoids undesirable reprogramming of the EEPROM. Clicking *EEPROM→ EEPROM lock* in the menu bar permanently locks the EEPROM. After locking the EEPROM, it cannot be unlocked.

After pressing the *Verify Register* button (also located in the menu bar), the current SMBus Interface setting is compared bit-wise with the CDCE906/CDCE706 control register that is connected to the PC. All bits of the control register that are different to the SMBus Interface setting are shown in a table. The bits, which show either 0 or 1, represent the control register setting of the CDCE906/CDCE706.

After the SSC settings were changed, PLL 2 must be reset by setting the PLL into bypass mode for a short time. This is done automatically by the SMBus interface.

Click *Programming Assistant* in the menu bar to switch to the *CDCE906-706 Programming Assistant*, which helps to create a setup for the CDCE906/CDCE706 by choosing the input and output settings.

### 4.1.3 Save/Load Setup

Saving and loading the setup of the *CDCE906-706 SMBus Interface* can be done in four different ways. Click *File*, and select one of the following options to save or load the current setup.

1. *Save Setup*/*Load Setup* - Saves/loads the setup as/from an encrypted file.
2. *Export *.txt*/*Import *.txt* - Exports/imports the setup as/from a text file. Use this format if you want to view the setup with a text editor later.
3. *Export *.csv*/*Import *.csv* - Exports/imports the setup as/from a comma-delimited file. Use this format if you want to view the setup with Microsoft™ Excel later
4. *Export Intel Hex *.hex/Import Intel Hex *.hex* - Exports/imports the setup as/from Hexadecimal Object File Format. Usually programmers can directly read-in this file format.
5. *Configuration Code Release Sheet* - Use this option if you want to order factory-programmed EEPROM specials of the CDCE906/CDCE706. Contact your regional marketing or sales representative for further information.

## *4.2 CDCE906-706 Programming Assistant*

The *CDCE906-706 Programming Assistant* is a useful feature, which creates a setup for the CDCE906 or the CDCE706. The setup can be transferred to the serial interface software, by selecting *Accept Setup*. Final setup adjustment and CDCE906/CDCE706 programming is done with the *CDCE906-706 SMBus Interface*.

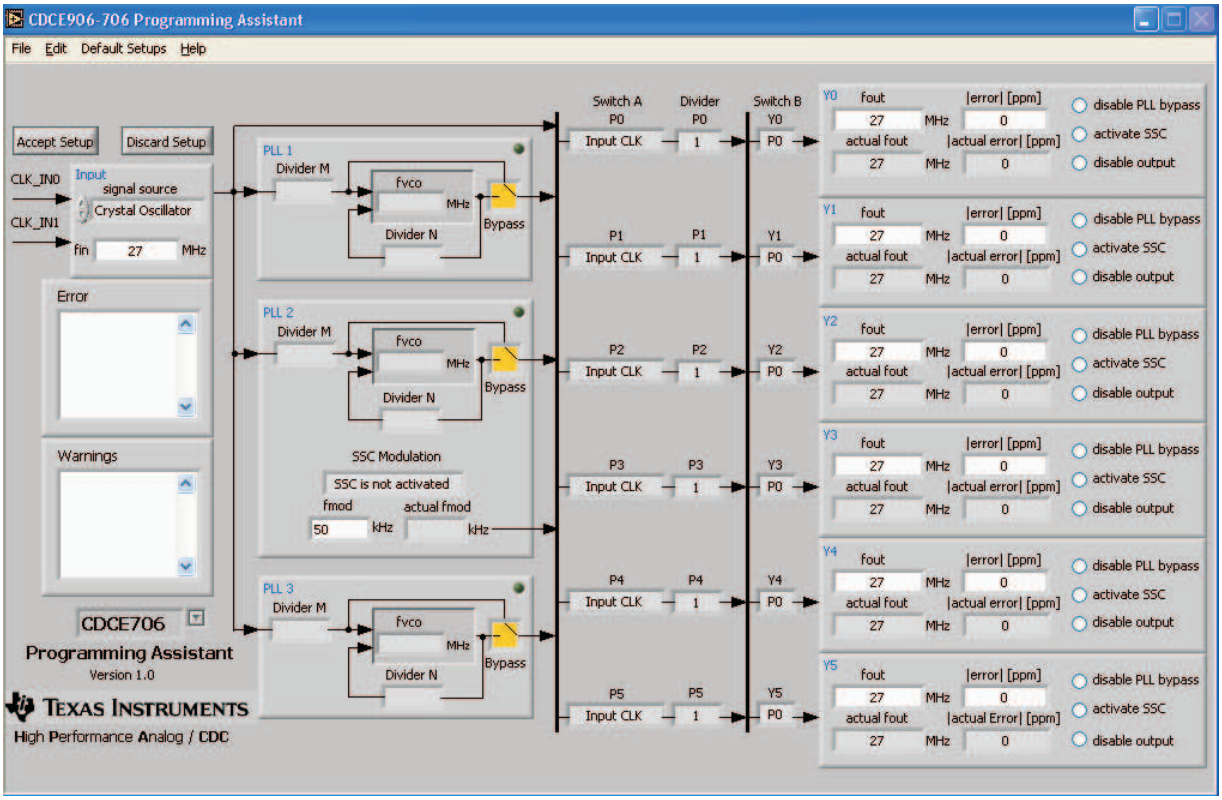


**Figure 4. Programming Assistant**

The Programming Assistant starts with its own default setup. The default setup of the Programming Assistant is different to the default setup of the CDCE906/CDCE706. This is why, the Programming Assistant has a simple startup setup, which makes it easy to create a new user-defined setup. From this default setup, different parameters can be edited to create a user setup. All dividers, the VCO frequency, the SSC modulation frequency, the switch A/B settings, as well as the actual output frequency, and the actual error of all outputs, are calculated by defining the following parameters:

| | |
|---|---|
| signal source | Choose among crystal oscillator, LVMOS, and differential clock source |
| fin | Choose from 1 MHz to 167/200 MHz for CDCE906/CDCE706 LVCMOS/differential input and from 8 MHz to 54 MHz for crystal oscillator |
| CDCE906/ CDCE706 Switch | Choose if a CDCE706 or a CDCE906 setup is provided |
| SSC Modulation | Choose between no modulation and different center and down-spread modulations provided by PLL 2 |
| fmod | Choose a modulation frequency for SSC; *actual fmod* shows the closest possible modulation frequency |
| fout | Choose the output frequency for Y0–Y5; *actual fout* displays the closest possible output frequency with an error in frequency smaller than \|*error*\| |
| error | Choose the maximum allowed error between fout and actual fout; *actual error* displays the error of current frequency *actual fout* |
| disable PLL bypass | If the input frequency is a multiple of fout, fout is derived directly from fin. Click *disable PLL bypass* if Yx should be derived from a PLL. |
| activate SSC | Choose which outputs will have SSC. All outputs with SSC activated must be derived from the same PLL. |

| | |
|---|---|
| disable output | Choose which outputs will be disabled. The *Switch A* will be set to input clock and P Divider will be set to 1 for each disabled output. |

An Error is displayed, if the setup cannot be provided by the CDCE906/CDCE706

A Warning is displayed if something in the setup needs special attention from the user.

The *Accept Setup* button transfers the setup to the *CDCE906-706 SMBus interface*, where an individual adjustment of the setup is possible. This function is blocked if an error in the setup occurs. *Discard Setup* returns to the SMBus Interface without transferring the setup.

## 4.3 Tutorial

This section contains a step-by-step tutorial for creating a user-defined setup and programming the CDCE906/E706. The 27-MHz crystal of the EVM is used for reference. A 64-MHz CPU clock, different audio sample clocks for 24-kHz audio rate, a 27-MHz clock for an MPEG/AC-3 Audio Dec, and an additional 60-MHz clock is provided. The tutorial contains instructions and comments explaining the functionality of the software.

**Step-by-step instruction:**

1. Start TI Pro-Clock™.
2. Select CDCE906/E706.
   - The *CDCE906-706 SMBus Interface* is started.
3. Select Programming Assistant in the menu bar.
   - The*CDCE906-706 Programming Assistant* is started.
4. Select CDCE906 Default Setting from Default Setup in the menu bar.
   - All Outputs are in use. All PLLs are in bypass mode.
5. Click *disable output* for Y1-Y5.
   - Only Y0 is in use. All PLLs are in bypass mode.
6. Set fout of Y0 to 64 MHz.
   - Y0 has an output frequency of 64 MHz; PLL 1 is set up automatically.
7. Click *disable output* for Y1.
8. Set fout of Y1 to 9.216 MHz.
   - Y1 is set to 9.216 MHz; PLL 2 in use by Y1.
9. Click *disable output* for Y2.
10. Set fout of Y2 to 18.432 MHz.
    - 18.432 MHz is set to Y2; PLL 1 is in use by Y1 and Y2 because Y1 and Y2 are derived from the same PLL (groups of outputs are preferred to a single output).
11. Click *disable output* for Y3.
12. Set fout of Y3 to 6.144 MHz.
    - Y1, Y2, and Y3 are derived by PLL 1.
13. Click *disable output* for Y4.
14. Set fout of Y4 to 27 MHz.
    - 27 MHz is provided to Y4 by the input clock; PLL 3 is still not in use.

The 27 MHz of Y4 can be provided by a PLL if additional jitter cleaning is necessary:

1. Click *disable PLL bypass* at Y4.
   - PLL3 now provides 27 MHz; additional jitter cleaning is possible.
2. Click *disable output* at Y5.
3. Set fout of Y5 to 60 MHz.
   - Error message *The error for fout of Y5 is not procurable!* appears; this is why no PLL is left to

derive 60 MHz for Y5.

4. Set *error* of Y5 to 50000 ppm.
   - Y5 now provides 59.4 MHz ; the error compared to 60 MHz is 10000 ppm.
5. Click *Accept Setup*.
   - The CDCE906-706 Programming Assistant is closing; the CDCE906-706 SMBus Interface opens, the setup of the Programming Assistant is transferred to the SMBus Interface.
6. Click *write*.
   - The SMBus interface transfers the setup to the CDCE906/E706.

### 4.4 Software Installation

To install the TI Pro-Clock™, perform the following steps:

1. Download TI Pro-Clock™ from www.ti.com.
2. Run program setup.exe.
3. Reboot your computer.
4. Run the Software from Start → Programs → Texas Instruments → TI Pro Clock.

## 5 FAQ

**The CDCE906/CDCE706 register cannot be programmed. What is wrong?**

Check if the parallel port is connected to your PC and your EVM. Check if correct voltage is applied. Check if the multiuse pins 1 and 2 are used as address bits. Set the correct address via J10 and J12 if this applies.

**There is coupling between neighboring outputs, if the output frequency is checked with a probe. Is this device related?**

No - the coupling comes from the socket, which is optimized for ease of use and not for signal integrity. Use the *CDCE906/CDCE706 Performance Evaluation Module* for signal integrity evaluation.

## 6 Parts List

**Table 1. Parts List**

| Quantity | Reference | Part | Manufacturer | Part Number |
|---|---|---|---|---|
| 4 | B1–B4 | STAND OFF | | |
| 4 | | SCREW | | |
| 1 | C1 | 22 µF | Murata | GRM32ER71A226KE20L |
| 1 | C2 | 10 µF | Murata | GRM31CR70J106KA01L |
| 1 | C3 | 1000 pF | Panasonic | ECJ-0EB1E102K |
| 4 | C4, C8, C11, C12 | 100 n | Panasonic | ECJ-0EB1A104K |
| 1 | C5 | 1 µF | Panasonic | ECJ-0EB0J105M |
| 1 | C6 | 10 n | Panasonic | ECJ-0EB1E103K |
| 2 | C7, C10 | 10 p | Panasonic | ECD-G0E100C |
| 1 | C9 | 1000 P | Panasonic | ECJ-0EB1E101K |
| 1 | D1 | GREEN | Fairchild Semi | QTLP651C-IG |
| 1 | J1 | PARALLEL PORT | SPC Technology | DB-25P-PCB |
| 1 | J2 | SMA | Johnson Comp | 142-0701-841 |
| 1 | J3, J4 | HDR3 | | Header 3 pos, 0.100 ctr |
| 2 | J5 | HDR4 | | Header 4 pos, 0.100 ctr |
| 1 | L1 | 75 Ω at 100 MHz | Murata | BLM31PG500SN1L |

**Table 1. Parts List (continued)**

| Quantity | Reference | Part | Manufacturer | Part Number |
|---|---|---|---|---|
| 1 | P1 | PWR_IN | SPC Technologies | 845R |
| 1 | P2 | GND | SPC Technologies | 845B |
| 1 | R1 | 10K | Panasonic | ERJ-2RKF1002X |
| 1 | R2 | Not used | | |
| 4 | R3, R4, R7, R8 | 100 | Panasonic | ERJ-2GEJ101X |
| 4 | R5, R6, R9, R18 | 10K | Panasonic | ERJ-2RKF1002X |
| 4 | R10, R11, R14, R15 | 1K | Panasonic | ERJ-2RKF1001X |
| 2 | R12, R16 | 100 | Panasonic | ERJ-2RKF1000X |
| 2 | R13, R17 | 100K | Panasonic | ERJ-2RKF1003X |
| 6 | TP0–TP5 | Not used | | |
| 1 | U1 | SN74LV125 | TI | SN74LV125AD |
| 1 | U2 | CDCE906/CDCE706 | | ENPLAS OTS-20(28)-0.65-01 |

# 7 Board Layout and Schematic

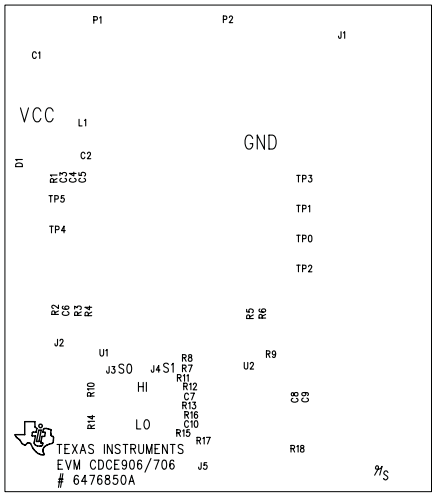


**Figure 5. Top Silkscreen**

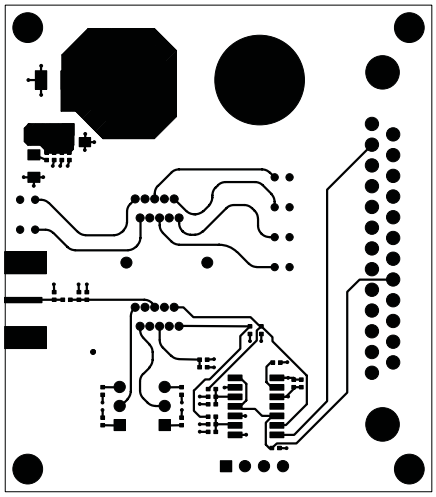

**Figure 6. Top Signal**

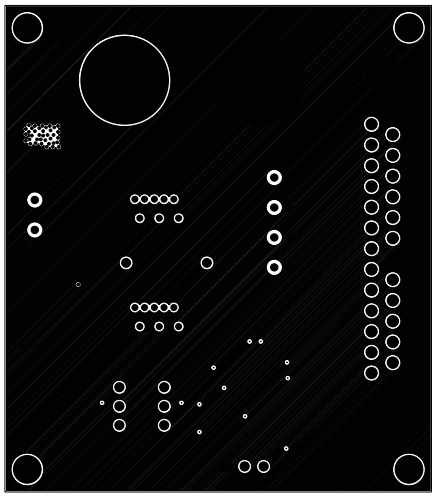

**Figure 7. GND Layer 2**

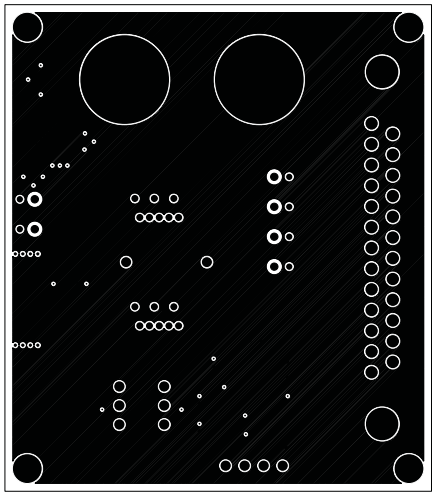

**Figure 8. VCC Layer 3**

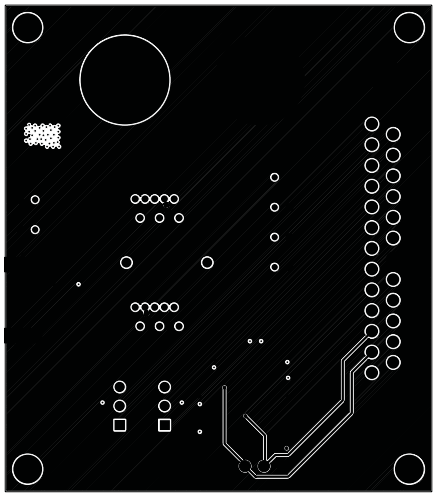

**Figure 9. Bottom Layer**

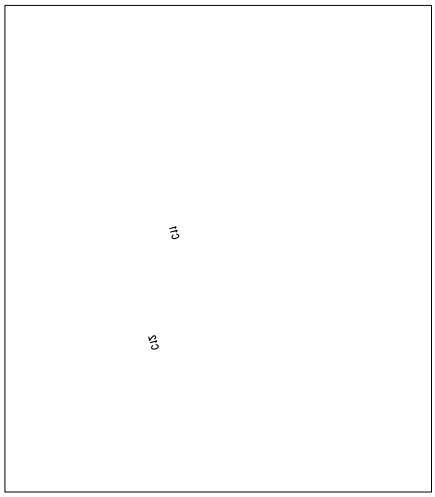

**Figure 10. Bottom Silkscreen**

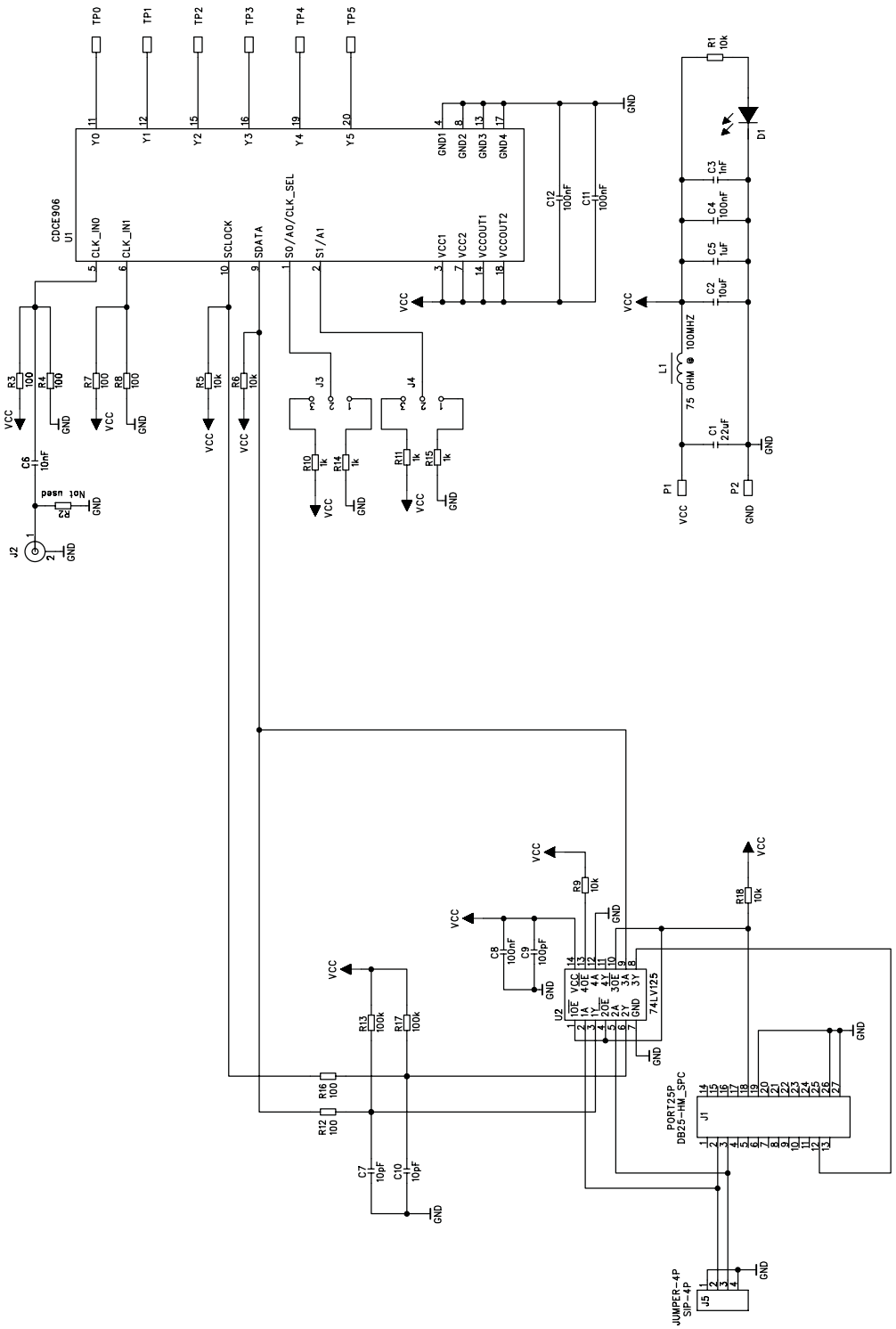


**Figure 11. Schematic**

## EVALUATION BOARD/KIT IMPORTANT NOTICE

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## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 3.6 V and the output voltage range of 3 V to 3.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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